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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,295	WOOD ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25, 26, 28 - 34 and 39 - 56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25, 26, 28 - 34 and 39 - 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on April 14, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 25, 26, 28, 30, 31 and 47 – 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoon et al. '887.

Regarding claim 25, Yoon et al. discloses in e.g., Fig. 13 a semiconductor device package (1), comprising:

- a semiconductor device (3) having diced edges;
- a dielectric substrate (19) having diced edges;
- a metal layer (12) having diced edges;
- a ball grid array (60) on said dielectric substrate, said dielectric substrate and said metal layer being located between said semiconductor device and said ball grid array; and

- electrical connections (40 and the structure between the solder ball 60 and the element 13) between said semiconductor device and said ball grid array,
- wherein said metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and metal layer edges, so as to provide said package with aligned edges.

Furthermore, the element 10 in Yoon et al. includes a metal layer 12 (column 17, line 23 – 28) and a dielectric substrate 19 and the element 10 is attached to a semiconductor wafer. Since the semiconductor wafer, the dielectric substrate, and the metal layer are diced simultaneously so as to provide said package 1 with aligned edges (see Fig. 13), it is held that the metal layer 12 inherently have a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and metal layer edges, so as to provide said package with aligned edges.

Regarding claim 26, Yoon et al. discloses in e.g., Fig. 13 and column 19, lines 53 – 58 said metal layer providing a ground plane (28) for said electrical connections.

Regarding claim 28, Yoon et al. discloses in e.g., Fig. 13 said metal layer (12) being arranged to dissipate heat from said semiconductor device.

Regarding claim 30, Yoon et al. discloses in e.g., Fig. 13 said connections (40 and the structure between the solder ball 60 and the element 13) comprising wire bonds.

Regarding claim 31, Yoon et al. discloses in e.g., Fig. 13 said connections (40 and the structure between the solder ball 60 and the element 13) comprising conductive vias (the structure between the solder ball 60 and the element 13).

Regarding claim 47, Yoon et al. discloses in e.g., Fig. 13 a semiconductor structure comprising:

- a plurality of semiconductor chips (3) formed on a wafer (wafer in Fig. 11A);
- a plurality of ball grid arrays (60) mounted on a dielectric substrate (18) such that said plurality of ball grid arrays face away from said wafer, each ball grid array respectively associated with one of said plurality of semiconductor chips on said wafer;
- electrical connections (12, 40 and 4) between each ball grid array and an associated semiconductor chip; and
- a first metal layer (12) attached (by adhesive layer 30 and the element 18) to the semiconductor wafer, said metal layer having sufficient stiffness to enable simultaneous dicing of said wafer, said dielectric substrate, and said metal layer.

Furthermore, the element 10 in Yoon et al. includes a metal layer 12 (column 17, line 23 – 28) and a dielectric substrate 19 and the element 10 is attached to a semiconductor wafer. Since the semiconductor wafer, the dielectric substrate, and the metal layer are diced simultaneously so as to provide said package 1 with aligned edges (see Fig. 13), it is held that the metal layer 12 inherently have a sufficient stiffness to enable simultaneous dicing of said wafer, said dielectric substrate, and said metal layer.

Regarding claim 48, Yoon et al. discloses in e.g., Fig. 13 the dielectric substrate comprising a thin, flexible film (18; column 10, line 42 – 49).

Regarding claim 49, Yoon et al. discloses in e.g., Fig. 13 the dielectric substrate comprising polymide (column 10, lines 43 – 44).

Regarding claim 50, Yoon et al. discloses in e.g., Fig. 13 the electrical connections comprising a wire bonds (40).

4. Claims 25 and 28 - 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Heo '689.

Regarding claim 25, Heo discloses in e.g., Fig. 6 a semiconductor device package, comprising:

- a semiconductor device (10) having diced edges;
- a dielectric substrate (22, at the top) having diced edges;
- a metal layer (21) having diced edges;
- a ball grid array (60) on said dielectric substrate, said dielectric substrate and said metal layer being located between said semiconductor device and said ball grid array; and
- electrical connections (40) between said semiconductor device and said ball grid array,
- wherein said metal layer has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and metal layer edges, so as to provide said package with aligned edges.

Furthermore, Heo clearly shows in e.g., Fig. 3g and column 4, lines 41 – 46 to cut the dielectric substrate edges and the metal layer edges according to the semiconductor device edges, so as to provide said package with aligned edges. Thus, it is held that Heo's metal layer inherently have stiffness sufficient to enable simultaneous dicing of said semiconductor device

edges, said substrate edges, and said metal layer edges, so as to provide said package with aligned edges.

Regarding claim 28, Heo discloses in column 3, lines 45 and 46 said metal layer (21) being arranged to dissipate heat from said semiconductor device.

Regarding claim 29, Heo discloses in column 3, line 5 said metal layer (21) comprising copper.

Regarding claim 30, Heo discloses in e.g., Fig. 6 said connections (40) comprising wire bonds.

Regarding claim 31, Heo discloses in e.g., Fig. 6 said connections (40) comprising conductive vias (the bottom place of solder ball in layer 24).

Regarding claim 32, Heo discloses in e.g., Fig. 6 said connections (40) further comprising conductive traces (23) on opposite sides of said substrate.

Regarding claim 33, Heo discloses in e.g., Fig. 6 a semiconductor device package, further comprising solder bumps (11) on said semiconductor device, said bumps connected to said traces.

Regarding claim 34, Heo discloses in e.g., Fig. 6 an insulative solder mask (24) for covering said dielectric substrate

5. Claims 40, 41, 43 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Hideshima et al. '865.

Regarding claim 40, Hideshima et al. discloses in e.g., Fig. 2 a semiconductor device package, comprising:

- a semiconductor device (11) having diced edges;
- a dielectric substrate (14) having diced edges over an upper side of said semiconductor device;
- a first metal layer (16) having diced edges below a lower side of said semiconductor device;
- a ball grid array (18B and 18E) over said dielectric substrate and on an opposite side of said dielectric substrate than said semiconductor device; and
- electrical connections (15B and 15E) between said semiconductor device and said ball grid array.

Regarding claim 41, Hideshima et al. discloses in e.g., Fig. 8 and column 6, lines 4 – 7 said first metal layer (16) has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said first metal layer edges, so as to provide said package with aligned edges. Furthermore, the element 16 in Hideshima et al. is a metal layer and is attached to a semiconductor wafer that has a dielectric substrate 14 thereon. Since the semiconductor wafer, the dielectric substrate, and the metal layer are diced simultaneously so as to provide said package 1 with aligned edges (see Fig. 2), it is held that the metal layer 16 inherently have a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said first metal layer edges, so as to provide said package with aligned edges.

Regarding claim 43, Hideshima et al. discloses in e.g., Fig. 8 a second metal layer (18C) below a lower side of said first metal layer and on an opposite side of said first metal layer from said semiconductor device.

Regarding claim 46, Hideshima et al. discloses in e.g., Fig. 8 and column 6, lines 4 – 7 the second metal layer having diced edges aligned with edges of said first metal layer, said semiconductor device edges, and said dielectric substrate edges.

6. Claims 47 – 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Horiuchi et al. '553.

Regarding claim 47, Horiuchi et al. discloses in e.g., Figs. 4(a) – 4(f), Figs. 5(a) – (5c), Fig. 6 and column 4, lines 39 – 67 a semiconductor structure comprising:

- a plurality of semiconductor chips (10) formed on a wafer (60);
- a plurality of ball grid arrays (26) mounted on a dielectric substrate (34) such that said plurality of ball grid arrays face away from said wafer, each ball grid array respectively associated with one of said plurality of semiconductor chips on said wafer;
- electrical connections (20, 14, 22, 32 and 28) between each ball grid array and an associated semiconductor chip; and
- a first metal layer (22) attached to the semiconductor wafer by the element 14, said metal layer having sufficient stiffness to enable simultaneous dicing of said wafer, said dielectric substrate, and said metal layer (the element 62 contains a metal layer 22, the dielectric substrate 34 and this claim doesn't claimed that the metal layer has a diced edge. Thus, the cut line 64 simultaneous dicing of said wafer, said dielectric substrate, and said metal layer).

Furthermore, the element 62 in Horiuchi et al. includes a metal layer 22 and a dielectric substrate 34 and the element 62 is attached to a semiconductor wafer 60. Since the semiconductor wafer, the dielectric substrate, and the metal layer are diced simultaneously (see Fig. 5c) so as to provide said package 12 with aligned edges (see Fig. 6), it is held that the metal layer 22 inherently have a sufficient stiffness to enable simultaneous dicing of said wafer, said dielectric substrate, and said metal layer.

Regarding claim 48, Horiuchi et al. discloses in e.g., Fig. 6 the dielectric substrate (34) comprising a thin, flexible film (compare to the wafer).

Regarding claim 49, Horiuchi et al. discloses in e.g., Fig. 6 the dielectric substrate comprising a polymide (column 4, line 63).

Regarding claim 50, Horiuchi et al. discloses in e.g., Fig. 6 the electrical connections comprising ball pads (20).

Regarding claim 51, Horiuchi et al. discloses in e.g., Fig. 6 a second metal layer (28) surface connected to the first metal layer (by the element 32).

Regarding claim 52, Horiuchi et al. discloses in e.g., Figs. 4(a) – 4(f), Figs. 5(a) – (5c), Fig. 6 and column 4, lines 39 – 67 a semiconductor device package, comprising:

- a semiconductor device (10) having at least one flip chip bump (14) contact;
- a dielectric substrate (34) having a via (32), said via being filled with a conductive material (Fig. 8b2);
- a ball grid array (26) mounted on said dielectric substrate, said dielectric substrate being located between said semiconductor device and said ball grid array; and

- a metal layer (22) having attached to the semiconductor device (by the element 14), said metal layer having sufficient stiffness to enable the simultaneous dicing of said dielectric substrate and said semiconductor device (10) from a structure comprising a wafer (60) and a dielectric substrate layer (34) attached thereto (se Fig. 5c).

Furthermore, the element 62 in Horiuchi et al. includes a metal layer 22 and a dielectric substrate 34 and the element 62 is attached to a semiconductor wafer 60. Since the semiconductor wafer, the dielectric substrate, and the metal layer are diced simultaneously so as to provide said package 12 with aligned edges (see Fig. 6), it is held that the metal layer 22 inherently have sufficient stiffness to enable the simultaneous dicing of said dielectric substrate.

Regarding claim 53, Horiuchi et al. discloses in e.g., Fig. 6 circuit traces (28 and 24) on the surface of the dielectric substrate, for electrically connecting the ball grid array mounted on the dielectric substrate to the semiconductor device.

Regarding claim 54, Horiuchi et al. discloses in e.g., Fig. 6 the circuit traces comprising at least an interior trace patterned (24) on a top surface of the dielectric substrate and at least one exterior trace (28) patterned on the bottom surface of the substrate.

Regarding claim 55, Horiuchi et al. discloses in e.g., Fig. 6 at least one interior trace (24) being in contract with at least one flip chip bump (14) on the surface of the semiconductor device (10) and said at least one exterior trace (28) being connected to said at least one interior trace through the conductively filled via (32).

Regarding claim 56, Horiuchi et al. discloses in e.g., Fig. 6 and column 8, lines 43 – 45 the conductively filled via (32) having a diameter within the range of approximately 25 microns to approximately 200 microns.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heo in view of Tuckerman et al. '539.

Heo discloses the claimed invention except for said metal layer providing a ground plane for said electrical connections. However, Tuckerman et al. teaches in e.g., Fig. 3 and column 4, lines 32 - 52 that a metal layer (44) providing a ground plane for an electrical connections. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Heo by using the metal layer as the ground plane for an electrical connections as taught by Tuckerman et al. The ordinary artisan would have been motivated to modify Heo in the manner described above for at least the purpose of providing a pinhole-free capacitor dielectric and improving electrical performance (column 4, lines 39 - 52).

9. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heo in view of Saitoh et al. '084.

Heo discloses the claimed invention except for said metal layer having a thickness within the range of "about" 0.13 millimeters to "about" 0.25 millimeters. However, Saitoh et al. teaches

in e.g., Fig. 3, column 2, lines 60 - 62 and column 3, line 51 that a metal layer (5B) having a thickness of from 5 μm to 150 μm which is within the range of "about" 0.13 millimeters to "about" 0.25 millimeters. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Heo by using the range of the thickness for the metal layer as taught by Saitoh et al. The ordinary artisan would have been motivated to modify Heo in the manner described above for at least the purpose of increasing electrical communication.

10. Claims 42 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hideshima et al. in view of Saitoh et al. '084.

Hideshima et al. discloses the claimed invention except for said first and/or second metal layer having a thickness within the range of "about" 0.13 millimeters to "about" 0.25 millimeters. However, Saitoh et al. teaches in e.g., Fig. 3, column 2, lines 60 - 62 and column 3, line 51 that a metal layer (5B) having a thickness of from 5 μm to 150 μm which is within the range of "about" 0.13 millimeters to "about" 0.25 millimeters. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Hideshima et al. by using the range of the thickness for the first and/or second metal layer as taught by Saitoh et al. The ordinary artisan would have been motivated to modify Hideshima et al. in the manner described above for at least the purpose of increasing electrical communication.

11. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hideshima et al. in view of Magdo et al. '148.

Hideshima et al. discloses the claimed invention except for said first metal layer having a thickness of "about" 0.00254 millimeters. However, Magdo et al. teaches in e.g., Fig. 1E and column 7, lines 12 - 15 that a metal layer (15) having a thickness of 2.5 μm which is "about" 0.00254 millimeters. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to specifically set Hideshima et al.'s metal layer thickness to be about 0.00254 mm as taught by Magdo et al. The ordinary artisan would have been motivated to modify Hideshima et al. in the manner described above for at least the purpose of reducing height of the semiconductor package.

Response to Arguments

12. Applicant's arguments filed on April 14, 2004 have been fully considered but they are either moot in light of the new grounds of rejection or are not persuasive.

On page 7, applicant argues "Yoon does not teach or suggest 'a metal layer ... [having] stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said metal layer edges, so as to provide said package with aligned edges,' as recited by claim 25." This argument is not persuasive because Yoon clearly shows in Fig. 6 and column 17, line 23 – 28 the element 12 is a metal layer and has metal layer edges that are formed by a simultaneous dicing the dielectric substrate, the metal layer and the semiconductor device so as to provide said package with aligned edges (see Fig. 13). Thus, it is held that the metal layer 12 inherently have a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said metal layer edges, so as to provide said package with aligned edges.

Further, applicant argues "Heo fails to disclose a metal layer having 'a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said substrate edges, and said metal layer edges, so as to provide said package with aligned edges,' as recited by independent claim 25" This argument is not persuasive. Heo clearly shows in e.g., Fig. 3g and column 4, lines 41 – 46 to cut the dielectric substrate edges and the metal layer edges according to the semiconductor device edges, so as to provide said package with aligned edges. Thus, it is held that Heo's metal layer inherently have stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said substrate edges, and said metal layer edges, so as to provide said package with aligned edges.

Finally, applicant argues "Hideshima does not teach or even suggest 'electrical connections between said semiconductor device and said ball grid array,' as recited by claim 40." This argument is not persuasive. Hideshima discloses in column 4, line 62 – column 5, line 26 the silicon substrate 11, which is a collector region, is electrically connected to the base region 12 that is electrically connected to the electrical connections (the elements 15B and 15E). Thus, Hideshima discloses the following limitation "electrical connections (15b and 15E) between said semiconductor device (11) and said ball grid array (18B and 18E) ".

For the above reasons, the rejection is maintained.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu

Examiner
Art Unit 2815

c.c.
7/9/04 2:41:53 PM

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800